Please cancel claims 8-11, 21 and 22, without prejudice.

Please add the following claims.

--23. (New) A method for providing an output signal with a characteristic frequency that is a first integer, N, multiple of a characteristic frequency of an input signal, said method comprising:

generating one or more oscillator signals with a characteristic frequency that is a second integer, M, multiple of the characteristic frequency of the output signal, wherein the one or more oscillator signals include a feedback signal;

dividing the characteristic frequency of the feedback signal by the first integer, N, factor and the second integer, M, factor;

comparing a phase or the frequency characteristic of the feedback signal to a phase or the frequency characteristic of the input signal; and

dividing the characteristic frequency of a particular one of the one or more oscillator signals by the second integer, M, factor thereby providing the output signal with the characteristic frequency that is the first integer, N, multiple, of the characteristic frequency of the input signal.

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24. (New) The method of claim 23, further comprising:

generating a voltage based on the comparison between the phase or the frequency characteristic of the feedback signal to the phase or the frequency characteristic of the input signal.

25. (New) The method of claim 23, wherein each of the one or more oscillator signals is associated with M phases of the characteristic frequency of the output signal.

26. (New) The method of claim 25, further comprising:

selecting the particular phase; and

selecting the particular one of the one or more oscillator signals, wherein the M phases associated with the particular one of the one or more oscillator signals includes the particular phase.

27. (New) A phase lock loop for providing an output signal with a characteristic frequency that is a first integer, N, multiple of a characteristic frequency of an input signal, said phase lock loop comprising:

a voltage controlled oscillator for generating one or more oscillator signals with a characteristic frequency that is a second integer, M, multiple of the characteristic

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frequency of the output signal, wherein the one or more oscillator signals include a feedback signal;

one or more divider circuits for dividing the characteristic frequency of a particular one of the one or more oscillator signals by the second integer, M, factor thereby providing the output signal with the characteristic frequency that is the first integer, N, multiple of the characteristic frequency of the input signal;

one or more divider circuits for dividing the characteristic frequency of the feedback signal by the first integer, N, factor, and the second integer, M, factor; and

a phase detector for comparing a phase or the frequency characteristic of the feedback signal to a phase or the frequency characteristic of the input signal.

28. (New) The phase lock loop of claim 27, further comprising:

a loop filter for generating a voltage based on the comparison between the phase or the frequency characteristic of the feedback signal to the phase or the frequency characteristic of the input signal.

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29. (New) The phase lock loop of claim 27, wherein each of the one or more oscillator signals is associated with M phases of the characteristic frequency of the output signal.

30. (New) The phase lock loop of claim 29, further comprising:

a multiplexer for selecting the particular phase; and

selecting the particular one of the one or more oscillator signals, wherein the M phases associated with the particular one of the one or more oscillator signals includes the particular phase.

31. (New) A phase lock loop for providing an output signal with a desired characteristic frequency that is an integer, N, multiple of a characteristic frequency of an input signal, said phase lock loop comprising:

a voltage controlled oscillator generating one or more oscillator signals, wherein each of the one or more signals are associated with M phases of the desired characteristic frequency of the output signal; and

a phase detector for comparing a phase or the frequency characteristic of the input signal to a phase or frequency characterstic of a particular one of the one or more oscillator signals to the input signal.

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32. (New) The phase lock loop of claim 31, further comprising:

a multiplexer for selecting an output signal from the one or more oscillator signals; and

a divider circuit for reducing a characteristic frequency of the output signal to the desired characteristic frequency.

33. (New) The phase lock loop of claim 32, wherein the multiplexer selects a particular phase, and wherein the M phases associated with the selected output signal from the one or more oscillator signals includes the particular phase.

34. (New) The phase lock loop of claim 33, wherein the multiplexer selects the particular phase based on a Gray code.

35. (New) The phase lock loop of claim 33, further comprising:

one or more divider circuits for reducing the frequency of the output signal to the desired characteristic frequency, wherein the divider circuit reduces the frequency of the output signal by an integer, M, factor.

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36. (New) The phase lock loop of claim 35, further comprising:

one or more divider circuits for reducing the characteristic frequency of the particular one of the oscillator signals by an integer, M, factor and an integer, N, factor.

37. (New) The phase lock loop of claim 31, further comprising:

a loop filter for increasing or decreasing a characteristic frequency of the voltage controlled oscillator signals based on the comparison of the phase or frequency characteristic of the input signal to the phase or frequency characteristic of the particular one of the one or more reference clock signals by the detector.

38. (New) A phase lock loop for providing an output signal with an output frequency, wherein the output frequency is an integer, N, multiple of an input frequency of an input signal, said phase lock loop comprising:

an oscillator for generating an oscillator signal with an oscillator frequency;

a divider for reducing the oscillator frequency of the oscillator signal by an integer, M, factor thereby providing

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an output signal with the output frequency that is the integer, N, multiple of the input frequency;

a phase detector for comparing the input signal to a feedback signal, wherein the feedback signal has a frequency that is reduced from the oscillator frequency; and

wherein the integer, N, is a factor for reducing the oscillator frequency to the frequency of the feedback signal.

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